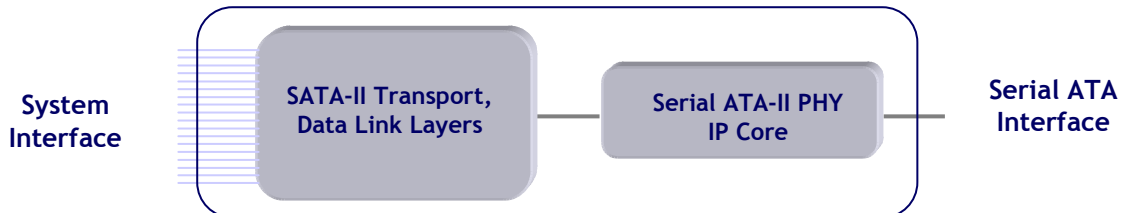




SATA-II PHY IP Core



Overview

The Aeluros SATA II IP core provides a complete PHY layer implementation for the SATA II 3.0 Gbps interface. Serial ATA II provides a comprehensive solution to the challenge of maintaining low system cost points in the face of increasing storage bandwidth. By making use of a robust 3.0 Gbps serial link, by incorporating SCSI-like features such as command queuing and backplane support, and by remaining software compliant with previous generations of ATA, the Aeluros Serial ATA II 3.0 Gbps solution is able to bring volume driven PC-based economies of scale to a wide variety of storage solutions. In addition, PHY-level compliance to the Serial Attached SCSI (SAS) specification enables further system flexibility. The Aeluros SATA II IP core provides an efficient, low-cost and low-power solution for SATA needs, and ensures a fast ramp to a robust silicon solution.

	Data Rate	Jitter 85C, 1.14V
SATA-II	3.0Gbps	0.24UI, 80ps
SATA-I	1.5Gbps	0.18UI, 119ps

Tx jitter measured from eye diagram of PRBS $2^{10}-1$ data and with a signal generator as the reference clock source.

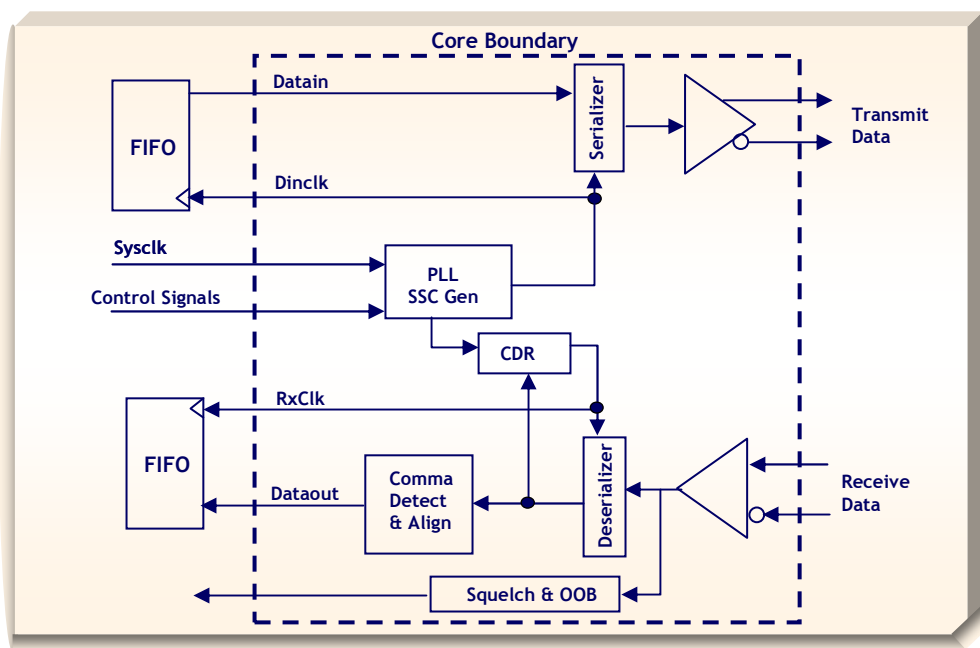
Features

- Compliant with SATA Spec Rev 1.0a
- Compliant with SATA II: PHY spec Rev 1.0
- SAPIs-compliant parallel interface
- TSMC 0.13mm (1.2V/2.5V) process
- Spread spectrum clocking support (RX)
- Transmit equalization (pre-emphasis)
- Programmable output swing
- Power down mode support
- Programmable termination resistor
- Out of band signaling
- Parallel & serial loopbacks
- Backwards compatible to 1.5Gbps
- Hot-plug capability
- Power consumption per channel - 80mW
- Compact size (.77x1.1mm, including I/Os)

Serial ATA II PHY IP Core

Applications

- Serial ATA Host Controllers
 - Serial ATA Device Controllers
 - Host Bus Adapters
- Server and PC Motherboards
 - RAID or JBOD Solutions
 - NAS, SAN, and DAS Systems
 - Serial ATA Add-in Cards



Development Package

All design, layout, and simulation files necessary to replicate the complete block are provided. Documentation material and characterization results of the verified core are also provided. Aeluros is open to a range of support and consulting models in order to facilitate incorporation and implementation of the core. This will typically incorporate initial design handoff efforts, followed by ongoing support during the integration process.

Benefits

- Compatibility with 1st generation SATA
- Common industry interface to Link Layer
- Reduced EMI to meet FCC Requirements
- Enables 30" backplane & cable designs
- Optimizes power consumption
- Includes active, partial & slumber modes
- Control signaling support

Implementation Details

The Serial ATA II 3.0 Gbps IP block is designed for use in a variety of high-volume 0.13- μm generic production process to ensure a low cost curve for end products. It makes use of a single 1.2-V power supply, and possesses minimal power consumption requirements.

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