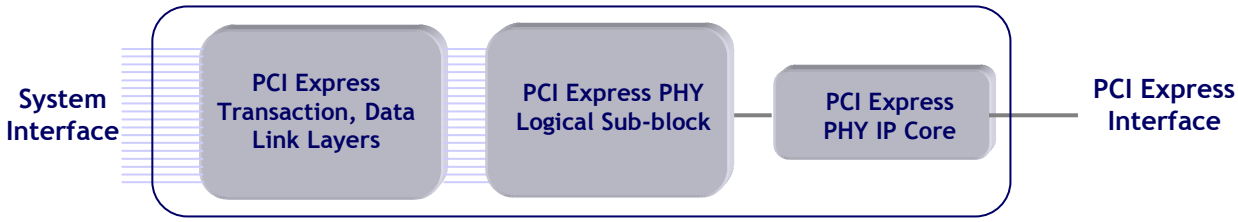
PCI Express PHY IP Core



Overview

The Aeluros PCI Express IP core provides a complete, reliable intellectual property solution for the electrical sub-block portion of the PCI Express physical layer. Support for 2.5 Gbps PCI Express signaling, with included spread spectrum clocking, beacon out-of-band signaling and de-emphasis support, ensures full compliance with the PCI Express standard and interoperability with solutions from other vendors. The Aeluros PCI Express solution enables a high-volume implementation at cost-points equivalent to or below the PCI cost structure while addressing a wide variety of applications from computing to storage to communications. Suitable for integration into complex silicon solutions, the Aeluros PCI Express IP core leverages Aeluros' low-power design expertise to achieve the optimal balance of power, performance and area efficiency.

	Data Rate	Jitter 85C, 1.14V
PCIE	2.5Gbps	0.18UI, 70ps

Tx jitter measured from eye diagram of PRBS 2^10-1 data and with a signal generator as the reference clock source

Features

- Compliant with PCIe base spec Rev 1.0a
- TSMC 0.13µm (1.2V/2.5V) process
- PIPE 1.0 compliant parallel interface
- Spread spectrum clocking support
- Programmable output swing
- Power down mode (P0, P0s, P1, P2)
- Programmable termination resistor
- Beacon out-of-band signaling
- Receiver detection sequence
- Receiver sensitivity ~ 65mV
- Max power = 92 mW/channel (P0)
- Parallel & serial loopbacks
- Compact design (.77 x 1.1mm, with I/Os)
- Hot-Plug capability
- Reference frequencies from 25 – 200MHz

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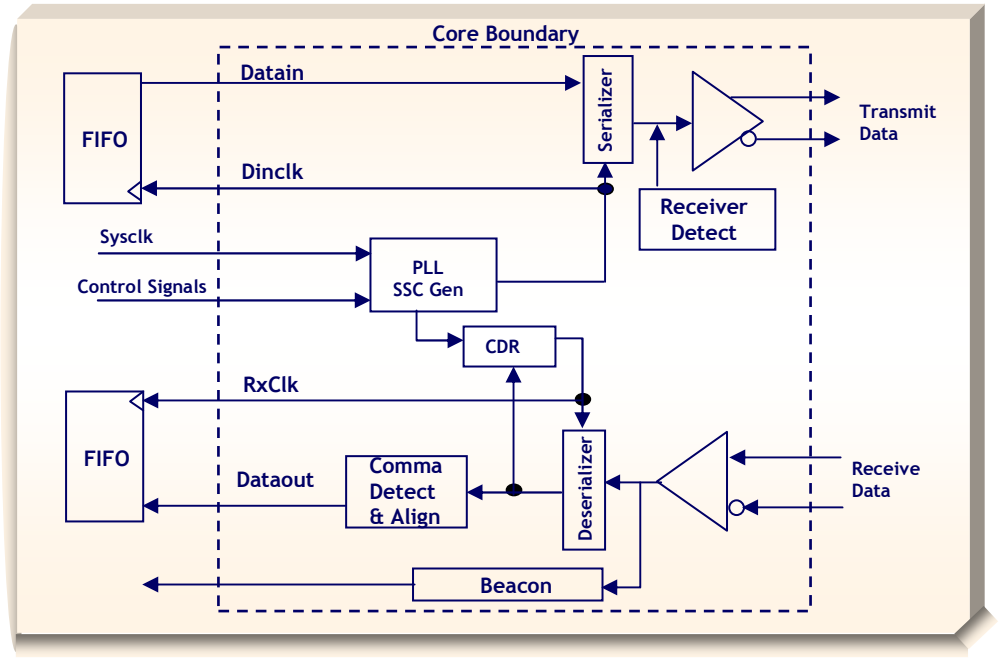
Applications

- PCI Express Host Bridge
- PCI Express End Point
- PCI Express Switch
- PC Chipset
- Serial ATA Bridge
- InfiniBand Bridge
- PCI – PCI Express Bridge
- PCI Express Add-in Card



Development Package

All design, layout, and simulation files necessary to replicate the complete block are provided. Documentation material and characterization results of the verified core are also provided. A full PIPE interface implementation is also included. Aeluros is open to a range of support and consulting models in order to facilitate incorporation and implementation of the core. This will typically incorporate initial design handoff efforts, followed by ongoing support during the integration process.

Implementation Details

The PCI Express IP block is designed for use in a variety of high-volume 0.13-mm generic production processes to ensure a low cost curve for end products. It makes use of a single 1.2-V power supply, and possesses minimal power consumption requirements.

Benefits

- High data rate with flexible bus widths & industry-standard interface to Link Layer
- Reduced EMI to meet FCC requirements
- Optimized power consumption
- Includes P0, P0s, P1, P2 modes
- Control signaling support
- Avoids invalid data transfer
- Enhances testability with minimized Silicon cost

ISO 9001:2000 registered

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