



Product Overview

The following chart shows the type of fundamental change that the emerging SFP+ modules will introduce to the architecture of the line card. As shown, the main functions of the 10G PHY, including the CDR function, the SerDes function and the electronic dispersion compensation function (EDC) - compliant with IEEE802.3aq specifications - will transition entirely to the line card and out of the optical modules. Consequently, systems designers - who until now could depend on the modules vendors to work out the complicated optical front end and simply receive an amplified, conditioned signal from the optical modules - have to deal with a whole new set of issues related to 10G serial signals. The stage is now set for a new group of IC vendors to fill the need with low-power, high performance 10G PHY devices.



Features

- Integrated, proprietary implementation of EDC functionality
- Equalizes pre-cursor, post-cursor & symmetric pulses - defined in IEEE 802.3aq (4-5 dB margin to spec at room temperature)
- Adaptive equalization based on FFE/DFE implementation
- Programmable bit & lane ordering
- Adjustable XAUI transmit pre-emphasis and receive equalization
- Jumbo frames supported (up to 20K bytes)
- Multiple loop-back modes
- Packet, PRBS, CJPAT & CRPAT generators & checkers
- 130 nm generic CMOS process



Applications

- SFP+ Optical Modules
 - Data Centers
- 10 Gigabit Ethernet LAN/ MAN/ SAN Systems
- 10GbE Add/drop Multiplexers
 - 10GbE Switch/router Backbones
- 10GbE Hubs and Repeaters
 - 10GbE/10Gb FC Test Equipment
- 10GbE Terabit Routers
 - 10GbE NICs

Puma AEL2003 SINGLE CHANNEL SFI/XFI 10G CDR/EDC for SFP+ applications

- Single channel 10GbE CDR/EDC for line-cards & NICs with SFP+ modules
- Same high-performance EDC engine implemented with FFE/DFE architectures on 10G RX port
- Pre-emphasis on 10G
- EDC engine passes all stress test pulses—as defined in IEEE802.3aq
- Programmable rise/fall times
- Built-in PRBS & BER Features
- EDC engine has proven interoperability with several SFP+ vendors

Puma AEL2005 SINGLE CHANNEL XAUI/SFI LAN PHY/SerDes w/EDC for SFP+ applications

- Single channel 10GbE PHY/SerDes (10 Gbps-XAUI) for line-cards & NICs with SFP+ modules
- Integrated EDC engine implemented with FFE/DFE architectures on 10G RX port
- Pre-emphasis on 10G
- EDC engine passes all stress test pulses—as defined in IEEE802.3aq
- Programmable rise/fall times
- Built-in PRBS & BER Features
- Adjustable XAUI transmit pre-emphasis for 40 inches of FR4 with 1 connector
- TX pre-emphasis on XAUI interface
- Programmable bit & lane ordering
- EDC engine has proven interoperability with several SFP+ vendors

Puma AEL2006 DUAL CHANNEL SFI/XFI 10G CDR/EDC for SFP+ applications

- Dual channel 10GbE CDR/EDC for line-cards & NICs with SFP+ modules
- Same EDC engine implemented with FFE/DFE architectures on 10G RX port
- Pre-emphasis on 10G
- EDC engine passes all stress test pulses—as defined in IEEE802.3aq
- Programmable rise/fall times
- Built-in PRBS & BER Features
- EDC engine has proven interoperability with several SFP+ vendors

Puma AEL2010 DUAL CHANNEL XAUI/SFI LAN PHY/SerDes w/EDC for SFP+ applications

- Dual channel 10GbE PHY/SerDes (10 Gbps-XAUI) for line-cards & NICs with SFP+ modules
- Integrated EDC engine implemented with FFE/DFE architectures on 10G RX port
- Pre-emphasis on 10G
- EDC engine passes all stress test pulses—as defined in IEEE802.3aq
- Programmable rise/fall times
- Built-in PRBS & BER Features
- Adjustable XAUI transmit pre-emphasis for 40 inches of FR4 with 1 connector
- TX pre-emphasis on XAUI interface
- Programmable bit & lane ordering
- EDC engine has proven interoperability with several SFP+ vendors



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